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A segmentation layout guarding technique to mitigate parasitic capacitance of integrated resistors

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Abstract Within integrated circuit design, parasitic capacitance associated with the realisation of a resistor can limit circuit performance for certain applications, such as the analogue-to-digital converter. In this paper, a segmentation guarding layout technique is introduced that offers the circumvention of the parasitic capacitance of integrated resistors. The segmentation guarding technique is demonstrated on both diffusion and polysilicon integrated resistors.

Keywords CMOS · Integrated resistor · Segmented layout guarding · Parasitic capacitance

1 Introduction

Passive components, such as integrated resistors, are key elements of analogue and mixed-signal integrated circuit (IC) systems. The designed impedance of such resistors are dependent on the doping level, the resistivity of process material and the layout dimensions. The electrical parasitic reactance associated with an integrated resistor of a given geometry varies with temperature and voltage offset [1, 2]. The temperature changes the mobility of carriers, built-in potential and the depletion width of the resistor and substrate. Voltage variation causes the change of mobility and the depletion width of the resistor body. In order to characterise integrated resistors, models have been proposed and studied over several years; the equivalent circuits of both the diffusion and polysilicon resistor are shown in Fig. 1 [3–6]. The 3-terminal models, including two nodes and a substrate terminal, yield an accurate electrical behavioural model which may be used when the substrate under the resistor area is not connected to the reference ground (conventional two-terminal resistor models always bias the substrate to the ground) [1]. These models are lumped approximations; in reality, the capacitance is distributed along the length of the resistor.

The diffusion resistor and polysilicon resistor are commonly used in IC design. As shown in Fig. 1(a), the model of a diffusion resistor consists of contact resistances (R_{xa} and R_{xb}), substrate resistance (R_{xt}), two p–n junction diode current sources (I_{ra} and I_{rb}) and parasitic capacitances (C_{ja} C_{jb} and C_{jc}). Such capacitances are dominated by the depletion junction capacitance [1]. Figure 1(b) shows the equivalent circuits for a polysilicon resistor; its parasitic capacitance C is dominated by the poly-oxide capacitance [3].

The impedance of these types of integrated resistors is reduced by the capacitive parasitic current at high frequencies. This current is proportional to the charging potentials across such capacitances. A shielding voltage with equal potential mitigates the capacitive reactance as no charge flow results.

2 Proposed segmentation guarding technique

In the IC platform, ratios of the resistance of integrated resistors may be easily implemented by conventional methods, such as matching and dummy structure layout techniques. However, the frequency response of IC resistors with conventional layout is dominated by the parasitic capacitance at high frequencies.

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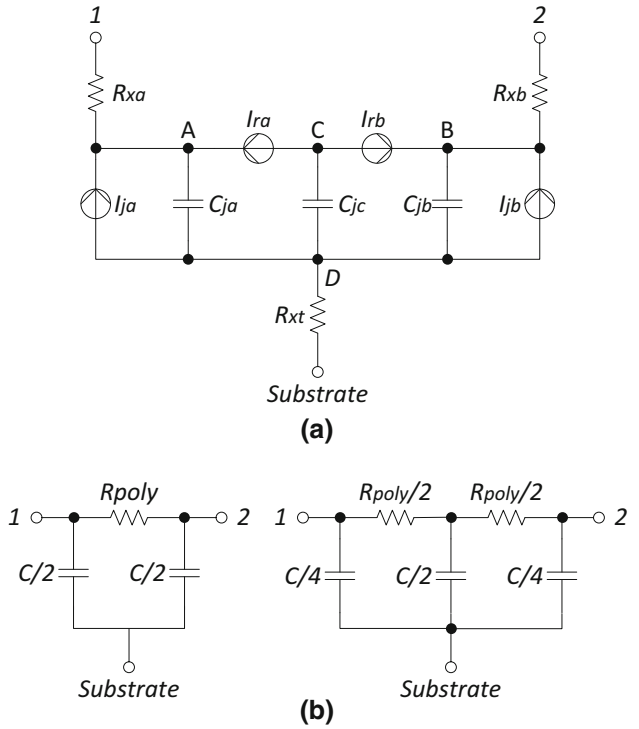

Fig. 1 **a** Equivalent circuit of a diffusion resistor. **b** Single-π and double-π equivalent circuit of a polysilicon resistor

The RF SPICE models of IC resistors, as given in Fig. 2, contain two types of parasitic capacitance; the stray capacitance of the resistor body (C_p) and resistor-to-substrate capacitance (C_s) [7].

For the simulation and analysis (Fig. 2), the input signal is applied at node 1 or 2 and the substrate is connected to ground (common terminal). The transfer function can be written as,

$$H(s) = \frac{sC_pR + 4}{sR(2C_p + C_s) + 8} \tag{1}$$

As the transfer function shows, the model has a pole and a zero in frequency domain. The zero is determined by the stray capacitance. The pole is controlled by both stray and resistor-to-substrate capacitance. In conventional IC design, C_s is a few orders larger than C_p. The approximate

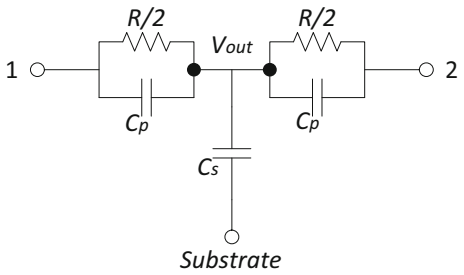

Fig. 2 RF SPICE models of IC resistors

frequency response of the model is illustrated in Fig. 3. The usable frequency range of the IC resistor is dominated by the pole. However, to increase this frequency range, both C_s and C_p need to be mitigated.

The slope of the roll-off for the pole, as demonstrated in Eq. (1), is determined by both C_s and C_p. An accurate ratio of the resistors is the key of common circuit performances, such as the instrumentation amplifier. In Fig. 4(a), (b), the frequency response of two polysilicon resistors, one each for 1 and 10 MΩ are depicted. The resistors are standard-layout, according to the AMS 0.35 μm process [7]. The simulation curves in Fig. 4 are plotted by Cadence Virtuoso [8].

The pole (f_{P1}) and zero (f_{Z1}) frequency for the 1 MΩ resistor are approximately located at 50 MHz and 5 GHz. For the 10 MΩ resistor, its pole (f_{P10}) and zero (f_{Z10}) frequency are around 10 and 500 MHz.

The ratio of these two resistors, as shown in Fig. 4(c), decreases at approximately 10 MHz (f_{P10}), which is determined by the 10 MΩ resistor due to its larger die area which brings about larger parasitic capacitance.

The derivative of resistor ratio is given in Fig. 4(d). It decreases between f_{P10} and f_{P1}, and is dominated by the 10 MΩ resistor. It then increases between f_{P1} and f_{Z10}, due to the impedance of both resistors reducing within this frequency range. When the frequency increases to 500 MHz (f_{Z1}), the rate of increasing lowers as the impedance of the 1 MΩ resistor becomes constant. Eventually, as shown in Fig. 4(c), (d), if the frequency is higher than both zeros of the resistors, in this frequency range the impedance ratio is dominated by the parasitic capacitance (or the die area of the resistor), which is not same as the designed resistance ratio. Hence, it is necessary to mitigate the parasitic capacitance of the IC resistors, especially for the large die area devices.

The traditional guarding, or shielding, technique which applies a guarding potential equal to the voltage at one end

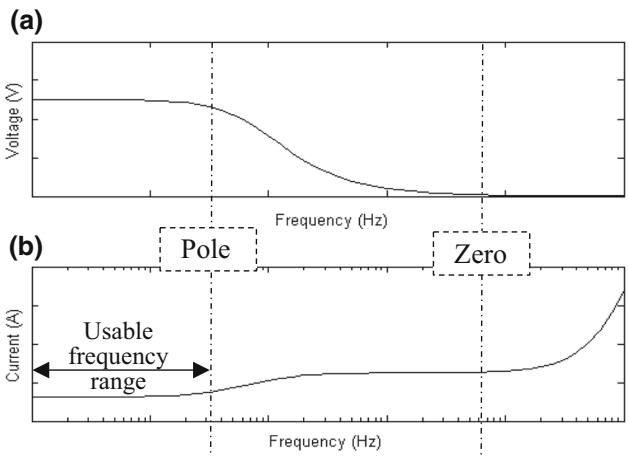

Fig. 3 Frequency response of integrated resistor RF SPICE models

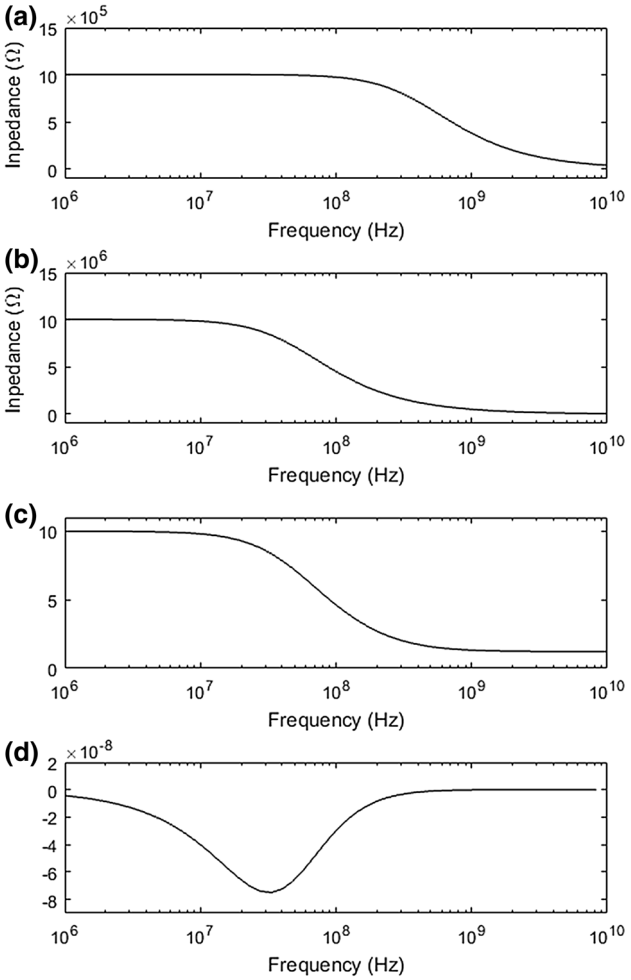

Fig. 4 Frequency response of **a** 1 MΩ polysilicon resistor. **b** 10 MΩ polysilicon resistor. **c** Ratio of resistors. **d** Derivative of resistor ratio

terminal of the resistor, is a commonly used layout technique to reduce the effect of parasitic capacitance [9–11]. However, a closer guarding voltage, with regards to the potential at a point along the resistor's length, will provide a better mitigation of the effect of parasitic capacitance.

This is most simply applied by providing the average of the terminals' voltage as the guarding potential. In Fig. 5, a resistor R has two node voltages, V_{N1} and V_{N2}, and its shield is connected to V_{shield}. Two node voltages, $V_{N1'}$ and $V_{N2'}$, are the buffered voltages of V_{N1} and V_{N2}, respectively. Also, as shown in Fig. 5, the two segmentation resistors R_a and R_b are equal, and are used as a pair to ensure the shielding voltage V_{shield} is the average of these buffered node voltages.

The voltage buffers are formed, as shown in Fig. 6, by low-noise two-stage Complementary Metal-Oxide Semiconductor (CMOS) operational amplifiers (OPAMPs) [12, 13]. In this study, the proposed circuits are targeted at IC implementation and simulated on the AMS 0.35 µm

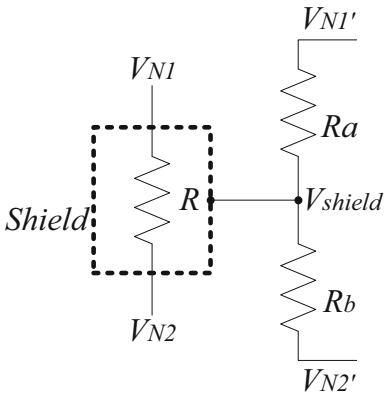

Fig. 5 Shielding with 1/2 voltage of the resistor

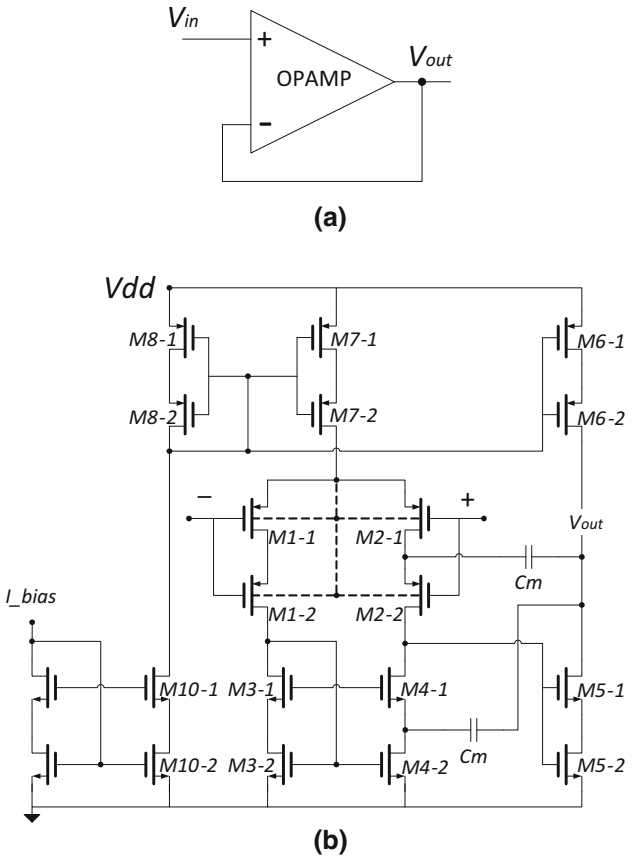

Fig. 6 Circuit schematic of **a** voltage buffer. **b** CMOS OPAMP

CMOS process [7]. The device geometries are given in Table 1.

Simple linear integration of the difference between the shield voltage and resistor voltage over length shows that the total charge on the parasitic capacitance is halved.

The precise bode plot of the OPAMP design is shown in Fig. 7. The frequency domain response of the OPAMP indicates that, it achieves circa a 58° phase margin and

Table 1 Dimension configurations of OPAMP

Device	Size
M1-1, M1-2, M2-1, M2-2	$4 \times \frac{100\,\mu m}{0.5\,\mu m}$
M3-1, M3-2, M4-1, M4-2	$1 \times \frac{20\,\mu m}{25\,\mu m}$
M6-1, M6-2, M8-1, M8-2	$1 \times \frac{10\,\mu m}{0.5\,\mu m}$
M7-1, M7-2	$1 \times \frac{20\,\mu m}{0.5\,\mu m}$
M5-1, M5-2	$1 \times \frac{2\,\mu m}{1\,\mu m}$
M9-1, M9-2, M10-1, M10-2	$1 \times \frac{10\,\mu m}{1\,\mu m}$
C_m	1.5 pF, $\frac{41.2\,\mu m}{41.2\,\mu m}$

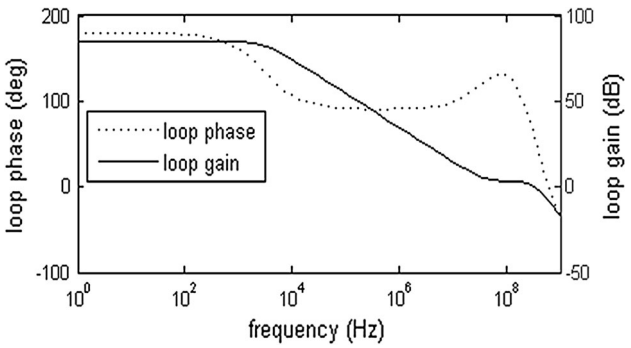

Fig. 7 Bode plot of OPAMP

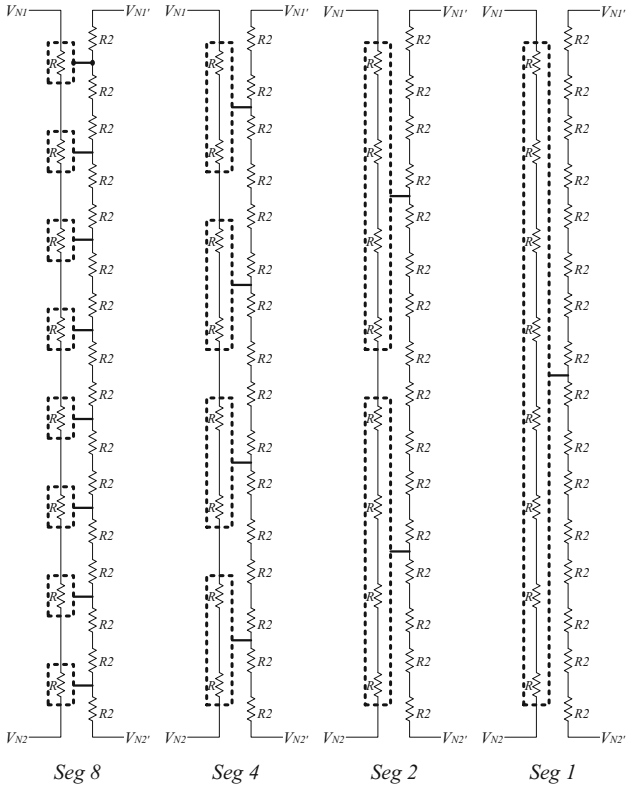

Fig. 9 Circuit schematic of SG techniques

5.4 dB gain margin. The bandwidth of the OPAMP is circa 3 kHz (3 dB).

The AC simulation of the voltage buffer is depicted in Fig. 8. It is able to track the input voltage up to 10 MHz which covers the frequency range of the simulated IC resistors.

For a large resistor, a more efficient Segmentation Guarding (SG) is employed by segmenting the long device into equal-length smaller resistors in series. A testbench is shown in Fig. 9, in which '*Seg 1*', '*Seg 2*', '*Seg 4*' and '*Seg 8*' indicate the number of target resistors employed. Each of the target resistors is guarded by a shield held at a potential tapped from a node providing the average voltage across that resistor.

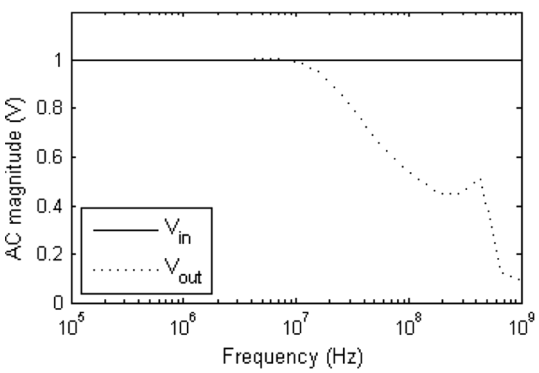

Fig. 8 AC simulation of voltage buffer

The impedance of the IC resistors (Z in Eq. 2) is reduced by the current into the parasitic capacitance at high frequencies,

$$Z = \frac{V_{in}}{I_r + I_p + I_s} \tag{2}$$

where, V_{in} the input voltage, I_r is the current into the resistance, I_p is the current into the capacitance C_p and I_s is the current into the capacitance C_s.

Without guarding, the current into stray capacitance (I_{p_no}) can be written as,

$$I_{p\_no} = \frac{V_{in} \cdot j\omega C_p}{2} \tag{3}$$

and, the current into the substrate capacitance (I_{s_no}) is,

$$I_{s\_no} = \sum_{i=1}^{n} \frac{V_{in} \cdot \left(\frac{n-i}{n} - \frac{1}{2}\right) \cdot j\omega C_s}{n} \tag{4}$$

where, n is the number of the potential SG resistor pairs.

When the SG is applied, the current into stray capacitance (I_{p_SG}) becomes,

$$I_{p\_SG} = \frac{V_{in} \cdot j\omega C_p}{n^2} \quad (5)$$

and, the current into the substrate capacitance (I_{s_SG}) is,

$$I_{s\_SG} \approx 0 \quad (6)$$

Therefore, as the equations show above, the SG can effectively reduce the current into parasitic capacitance, so that the usable frequency range of IC resistors are increased.

Without guarding, the power consumption for the IC resistors, both diffusion and polysilicon resistor, is about 50 μW. When the SG technique is implemented, the power consumption increases to circa 460 μW. The power for each voltage buffer, formed by the OPAMP, is approximately 210 μW. The power consumption of the OPAMP can be reduced by decreasing the biasing current.

3 Results

The testing configurations are given in Table 2. For both diffusion and polysilicon resistors, a relatively high overall resistance of 80 MΩ is selected, consisting of eight 10 MΩ resistors in series. The area of the diffusion resistors is larger, as the bulk resistivity is lower than the polysilicon, which leads to greater parasitic capacitance. For the SG resistors, sixteen 1 kΩ polysilicon resistors are used, to provide corresponding shielding voltages for both the diffusion and polysilicon resistors under test. A 'no guarding' test is also implemented as the benchmark. The device geometries of the IC resistors are given in Table 3.

The proposed SG technique is implemented on the AMS 0.35 μm CMOS process [7]. P-type diffusion resistors are used, and the N-wells underneath the target resistors held at the shielding potentials. As given in Table 2, five tests are carried out with different numbers of segmentations. A 1 V AC voltage is applied across the total target resistance in all tests, the corresponding AC currents are depicted in Fig. 10(a). At lower frequencies, the current through the target diffusion resistors of all tests are approximately equal. As the frequency increases, especially above 10 kHz, the current of the 'no guarding' test increases significantly, which is caused by the parasitic capacitive reactance. The impedance of the parasitic junction capacitance decreases with the increasing of frequency. The current into the target resistor is dominated by the parasitic capacitance at high frequencies. When the SGs are applied, the rate of increase of AC current with frequency decreases with increasing number of segmentations. As shown in Fig. 10(b), the calculated impedance indicates that, with

Table 3 Dimensions of IC resistors

Device	Size
R_{poly}	10 MΩ, $50 \times \frac{300\,\mu m}{2\,\mu m}$
R_{diff}	10 MΩ, $260 \times \frac{300\,\mu m}{1\,\mu m}$
R_{SG}	1 kΩ, $\frac{10\,\mu m}{10\,\mu m}$

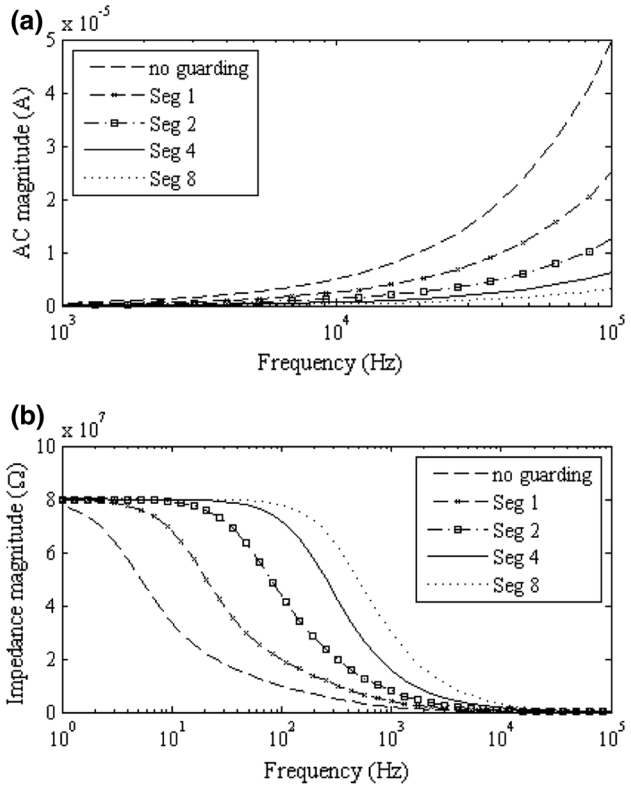

Fig. 10 **a** AC currents of diffusion resistors. **b** Impedance of diffusion resistors

Table 2 SG experiment configurations

Tests	Diffusion resistor		Poly resistor	
	Target resistors (MΩ)	SG resistors	Target resistors (MΩ)	SG resistors
No guarding	1 × 80	None	1 × 80	None
Seg 1	1 × 80	2 × 8 kΩ	1 × 80	2 × 8 kΩ
Seg 2	2 × 40	4 × 4 kΩ	2 × 40	4 × 4 kΩ
Seg 4	4 × 20	8 × 2 kΩ	4 × 20	8 × 2 kΩ
Seg 8	8 × 10	16 × 1 kΩ	8 × 10	16 × 1 kΩ

the SGs providing closer shielding voltages that track the distributed voltage along the length of the resistor, the parasitic capacitance of the target diffusion resistor is increasingly mitigated.

For the polysilicon resistor, the shielding voltages are also applied to the N-wells underneath the target resistors. As shown Fig. 11(a), the parasitic current generated by the capacitive reactance for the 'no guarding' test becomes noticeable when the frequency is above 500 Hz. The impedances of different tests are plotted in Fig. 11(b). It implies that the more SGs are implemented, the lesser the parasitic current; and, therefore, the more parasitic capacitance is circumvented.

A second on-chip testbench (TB) is implemented, as given in Fig. 12, an 80 MΩ polysilicon IC resistor is connected in series with a voltage buffer. The equivalent input impedance of the buffer is circa 42 GΩ [14]. The voltage across the resistor R_{ploly} is detected and amplified by the instrumentation amplifier,

$$V_{out} = A_{ins}(V_{in} - V_x)$$

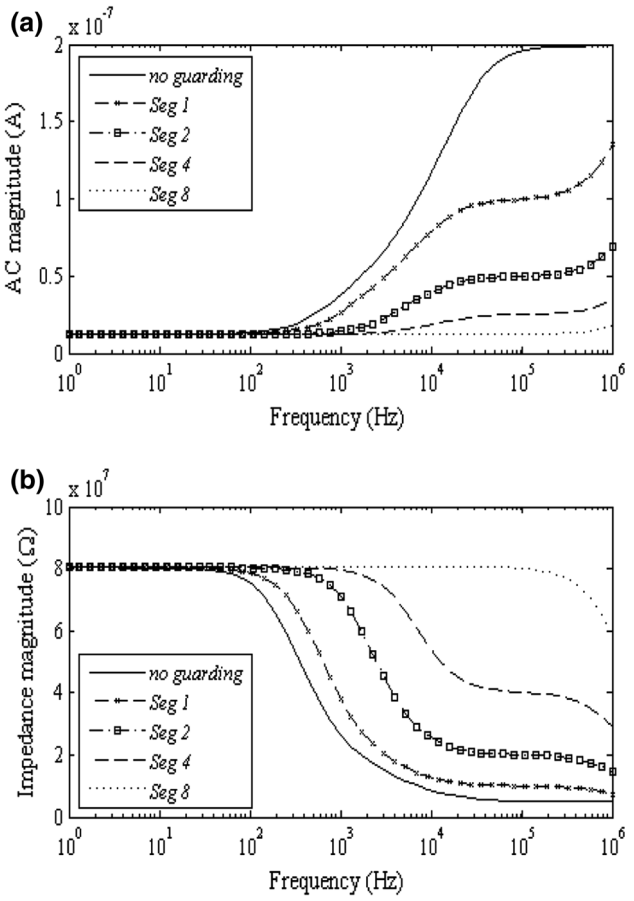

Fig. 11 **a** AC currents of polysilicon resistors. **b** Impedance of polysilicon resistors

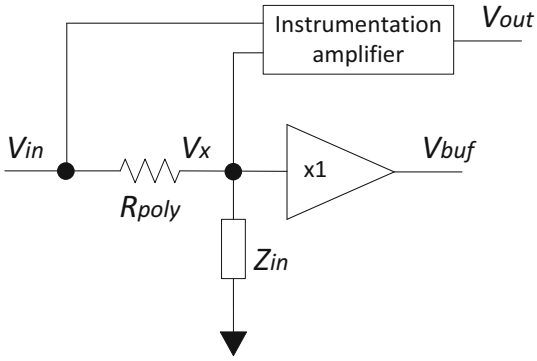

Fig. 12 On-chip TB of ploy resistor

where, V_{in} in the input voltage, V_x is the node voltage and A_{ins} is the gain of the instrumentation amplifier.

The experiment results are given in Fig. 13. The amplitude of the input signal is 100 mV, and the frequency is 1 kHz. The gain of the instrumentation amplifier is approximately 1.5 k. For the 'no guarding' test, as shown in Fig. 13(a), the output of the instrumentation amplifier is saturated. It is caused by the phase shift between V_{in} and V_x, which is determined by the capacitive reactance of the polysilicon resistor. When the SG technique (8 pairs of SG guarding resistors) is implemented, as shown in Fig. 13(b), the phase shift is significantly reduced, due to the effective circumvention of the parasitic capacitance.

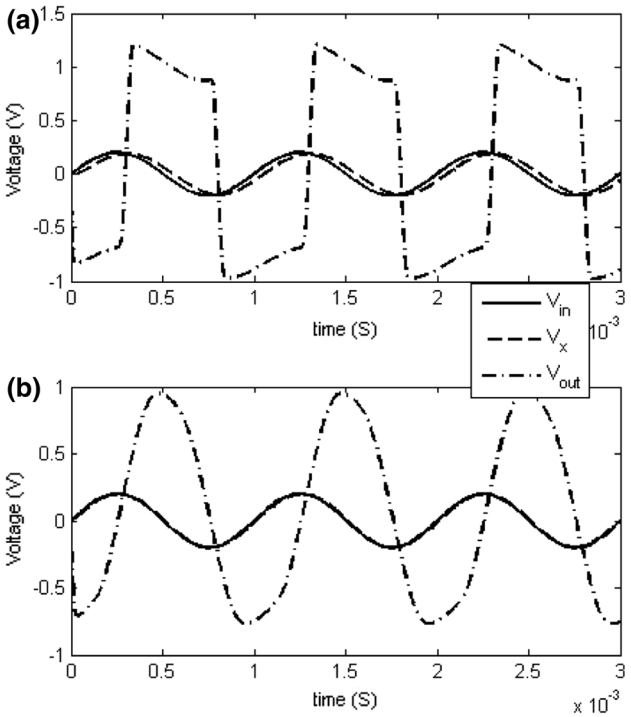

Fig. 13 Output of TB **a** Without SG. **b** With SG

An accurate measurement of the amplitude and phase difference for the IC resistor with different numbers of SG can be attained by implementing a suppression loop system [15].

4 Conclusion

A resistor segmentation layout guarding technique is demonstrated for IC implementation that offers better circumvention of parasitic capacitance than the conventional guarding technique. The key degree of freedom exploited is that a shield providing the average voltage, with respect to the end terminals' potential across the resistors' length offers a closer guarding voltage. The impedance of such resistors is dominated by the capacitive reactance at high frequencies. The usable frequency range of the IC resistor is limited by the large parasitic capacitance, using the conventional guarding technique.

By segmenting a long-length resistor into an increasing number of guarded devices, the die area of individual sub-devices is reduced. The parasitic capacitance of each smaller device, both stray capacitance of the resistor body and the resistor-to-substrate capacitance, is increasingly mitigated. This increases the usable frequency range of the integrated resistor. A concept-providing prototype is presented, and the simulated results indicate that a lower effective capacitive reactance of the integrated resistor is achieved by providing more SGs.

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